REMARKS / DISCUSSION OF ISSUES

Claims 1-8 are pending in the application. Claims 1 and 8 are the independent claims. Amendments to the claims are not made to overcome applied art. Rather, certain European-style phraseology and other required elements of European-style claims are replaced. No new matter is added.

Objection to the Specification

Amendments to the Abstract are believed to overcome the objections raised and add no new matter. Withdrawal of this objection is respectfully requested.

Rejections under 35 U.S.C. § 102

Claims 1-3, 6 and 8 are rejected under 35 U.S.C. § 102(b) as being anticipated by *Himeno* (US Patent 5,400,271). For at least the reasons set forth herein, Applicants respectfully submit that this rejection is improper and should be withdrawn.

At the outset Applicants rely at least on the following standards with regard to proper rejections under 35 U.S.C. § 102. Notably, a proper rejection of a claim under 35 U.S.C. § 102 requires that a single prior art reference disclose each element of the claim. *See, e.g., W.L. Gore & Assoc., Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 USPQ 303, 313 (Fed. Cir. 1983). Anticipation requires that each and every element of the claimed invention be disclosed in a single prior art reference. *See, e.g., In re Paulsen*, 30 F.3d 1475, 31 USPQ2d 1671 (Fed. Cir. 1994); *In re Spada*, 911 F.2d 705, 15 USPQ2d 1655 (Fed. Cir. 1990). Alternatively, anticipation requires that each and every element of the claimed invention be embodied in a single prior art device or practice. *See, e.g., Minnesota Min. & Mfg. Co. v. Johnson & Johnson Orthopaedics, Inc.*, 976 F.2d 1559, 24 USPQ2d 1321 (Fed. Cir. 1992). For anticipation, there must be no difference between the claimed invention and the reference disclosure, as viewed by a person of ordinary skill in the field of the invention. *See, e.g., Scripps Clinic & Res. Found. v. Genentech, Inc.*, 927 F.2d 1565, 18 USPQ2d 1001 (Fed. Cir. 1991).

Claim 1 is drawn to a data processing device for receiving an input stream of first data samples at a first rate and for generating an output stream of second data samples at a higher second rate by inserting additional data samples generated from said first data samples. The device features, inter alia:

"a) means for storing a predetermined one of said first data samples; and

b) means for adjusting the timing of said output stream, said time adjusting means comprising:

b1) means for skipping first predetermined ones of said second data samples derived from said stored predetermined one of said first data samples..."

Claim 8 includes similar features.

In rejecting claim 1, the Office Action directs Applicants to column 4, lines 39-50 and column 17, lines 10-18 for the alleged disclosure of means for skipping as recited in claim 1. However, there is no disclosure in these portions of the reference that disclose this subject matter. To wit, column 4, lines 39-50 disclose:

> Referring first to FIG. 1, there is shown a digital low-pass filter (LPF) to which an apparatus for calculating a sum of products according to the present invention is applied. The digital low-pass filter shown includes a data memory 1 into which input data of, for example, 16 bits inputted from an input terminal DI thereof are stored. The data memory 1 receives an address signal at an address terminal AD thereof and outputs data stored at an address designated by the address signal by way of an output terminal DO thereof to a latch circuit 2, an adder 3 and a switch 14. The latch circuit 2 receives, at a clock terminal CLK thereof, a clock signal having a period of 2/CK equal to twice a period of 1/CK (frequency CK) in which data are read out from the data memory 1, at a timing 16-bit data read out from the data memory 1 at a timing at which the clock signal is inputted.

Column 17, lines 10-18 disclose:

> At step S2, the data D_{-n} is latched by the register 35. Then at step S3, the sum of the data D_{-n} latched in the register 35 and the data D_n stored in the data memory 32, that is, $D_{-n}+D_n$, is calculated by the arithmetic and logic unit 36, and the sum is latched by the register 35. Then at step S4, the data $D_{-n}+D_n$ latched in the register 35 is latched by the register 37 and the mantissa part of the coefficient C_n stored in the coefficient memory 32 is latched by the register 40.

While the noted portions of the reference disclose various latching mechanisms, and data reading based thereon, there no disclosure of means for skipping *first*

predetermined ones of said second data samples. Thus, the applied art fails to disclose at least one feature of each of claims 1 and 8.

For at least the reasons set forth above, Applicants respectfully submit that a prima facie case of anticipation has not been established because the applied art fails to disclose at least one feature of each of claims 1 and 8. Therefore claims 1 and 8 are patentable over the applied art. Claims 2-7, which depend from claim 1, are patentable for at least the same reasons.

Rejections under 35 U.S.C. § 103

The rejections under this section of the Code have been considered. While in no way conceding the propriety of the rejections, at least because claims 4 and 5 depend from claim 1, these claims are patentable for at least the same reasons.

Conclusion

In view the foregoing, applicant(s) respectfully request(s) that the Examiner withdraw the objection(s) and/or rejection(s) of record, allow all the pending claims, and find the application in condition for allowance.

If necessary, the Commissioner is hereby authorized in this, concurrent, and further replies to charge payment or credit any overpayment to Deposit Account Number 50-0238 for any additional fees, including, but not limited to, the fees under 37 C.F.R. §1.16 or under 37 C.F.R. §1.17.

If any points remain in issue that may best be resolved through a personal or telephonic interview, the Examiner is respectfully requested to contact the undersigned at the telephone number listed below.

Respectfully submitted on behalf of:

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WSF

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